HD-QSFP28/100G-LR4

1 Features

1.1 Hot pluggable QSFP28 MSA formfactor
1.2 Compliant to IEEE802.3ba 100GBASE-LR4
1.3 Supports103.1Gb/s aggregate bit rate
1.4 Up to10km reach for G.652 SMF
1.5 Single +3.3V power supply
1.6 Operating case temperature:0~70°C
1.7 Transmitter: cooled 4x25Gb/s LANWDM DFB TOSA(1295.56,1300.05,1304.58,1309.14nm)
1.8 Receiver:4x25Gb/s PIN ROSA
1.9 4x25G electrical interface(OIFCEI-28G-VSR)
1.10 Maximum power consumption 4.0W
1.11 Duplex LC receptacle
1.12 RoHS-6 compliant

2 Applications

2.1 100GBASE-LR4 Ethernet Links
2.2 Infiniband QDR and DDR interconnects
2.3 Data center and Enterprise networking

3 General

This product is a 100Gb/s transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE 802.3ba standard. The module converts 4 input channels of25Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission .Reversely on the receiver side ,the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LANWDM DFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to10km links and compliant to optical interface with100GBASE-LR4 requirements specified in IEEE 802.3baClause88.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

4 Functional Description

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery(CDR)IC that reshapes and reduces the jitter of each electrical
signal. Subsequently, DFB laser driver IC converts each one of the 4channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled DFB lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE 802.3ba 100GBASE-LR4 requirements. These 4-lane optical signals will be optically multiplexed into a single fiber by a 4-to-1 optical WDM MUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or 2-wireserial interface.

The receiver receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by a1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value is reported through the 2-wire serial interface. Ifoneormorereceivedopticalsignalisweakerthanthethresholdlevel,RX_LOShardwarealarm will be triggered.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications themoduleoffers7lowspeed hardwarecontrolpins(includingthe2-wireserialinterface):ModSelL,SCL,SDA,ResetL,LPMode, Mod Prs Land IntL.

Module Select (Mod SelL) is an input pin. When held low by the host, this product responds to 2-wireserial communication commands. The Mod SelL allows the use of this product on a single 2-wire interface bus–individual Mod SelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of are set the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring are set.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system.The host identifies the source of the interrupt using the 2-wires erial interface.The IntL pin is an open collect or output and must be pulled to the HostVcc voltage on theHostboard.

5 Performance Specifications

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_{stg}	-40	+85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Operating relative humidity	RH	0	85	%
Supply Voltage	V_{CC}	-0.5	3.6	V
Damage Threshold, eachLane	THd	5.5		dBm

5.2 Recommended Operating Environment

Parameter	Symbol	Min.	Max.	Unit
Operating Case Temperature	T_C	0	+70	°C
Power Supply Voltage	V_{CC}	+3.135	+3.465	V
Data Rate,each Lane		25.78		Gb/s
Power Consumption	P		4.0	W
Supply Current	I_{CC}		1.21	A
Data Rate Accuracy	-	-100	100	ppm
Control Input Voltage High	-	-	2	V
Control Input Voltage Low	-	0.8	-	V
Link Distance with G652	-	-	10	km

5.3 Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Wavelength Assignment	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Transmitter						
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	PT			10.5	dBm	
Average Launch Power, Each Lane	PAVG	-4.3		4.5	dBm	
Extinction Ratio	ER	4			dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Damage Threshold, each Lane	THd	5.5			dBm	
Average Receive Power, Each Lane		-10.6		4.5	dBm	
Receiver Sensitivity,each Lane	SEN			-10.6	dBm	5.3.1
Receiver Reflectance	RR			-26	dBm	
LOSAssert	LOSA	-30			dBm	
LOSDeassert	LOSD			-13	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Note5.3.1:Measuredwith25.78GbpsPRBS231-1BER=5x10^{-5}.

5.4 Digital Diagnostic Functions

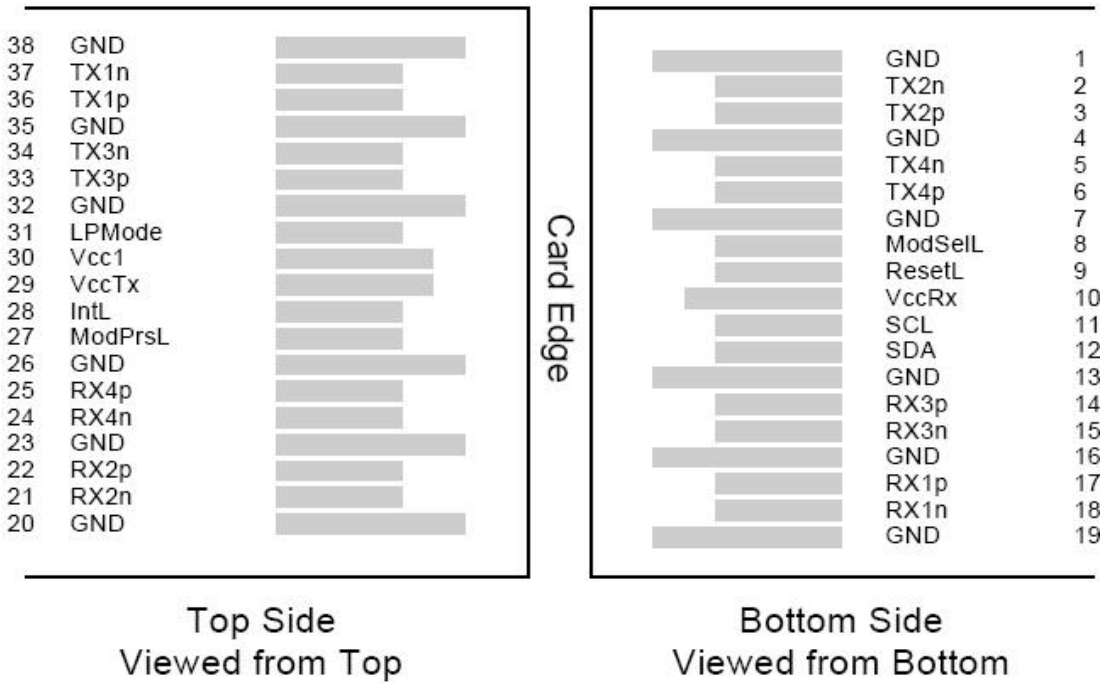
Parameter	Symbol	Min.	Max.	Unit	Note
Temperature monitor Absolute error	DMI_Temp	-3	+3	°C	Over operating Temperature range
Supply voltage monitor Absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RXpowermonitor Absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor Absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Duetomeasurementaccuracyofdifferentsinglemodefibers,therecouldbeanadditional+/-1dBfluctuation,or a+/- 3dB total accuracy.

6 Pin Definitions

6.1 Pin Diagram



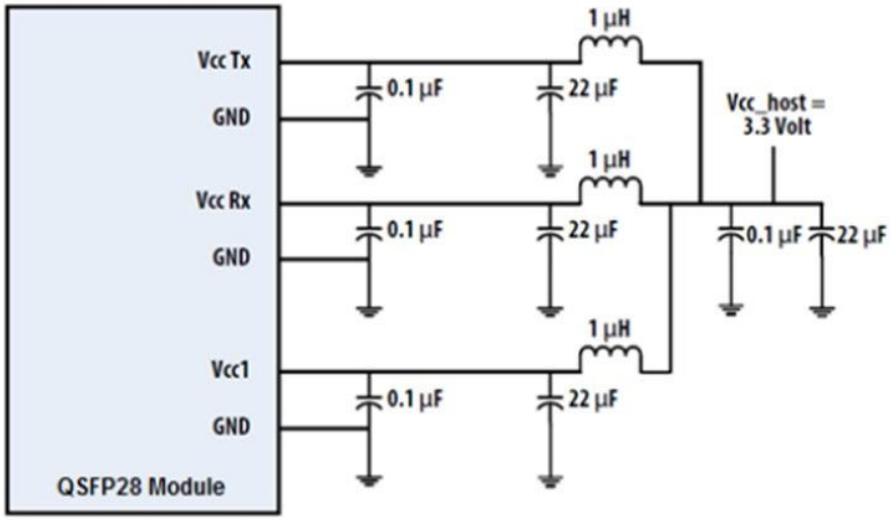
6.2 Pin Descriptions

Pin#	Logic	Name	Function	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes: Module circuit ground is isolated from module chassis ground within the module.GND is the symbol for signal and supply(power) common for QSFP28 modules.

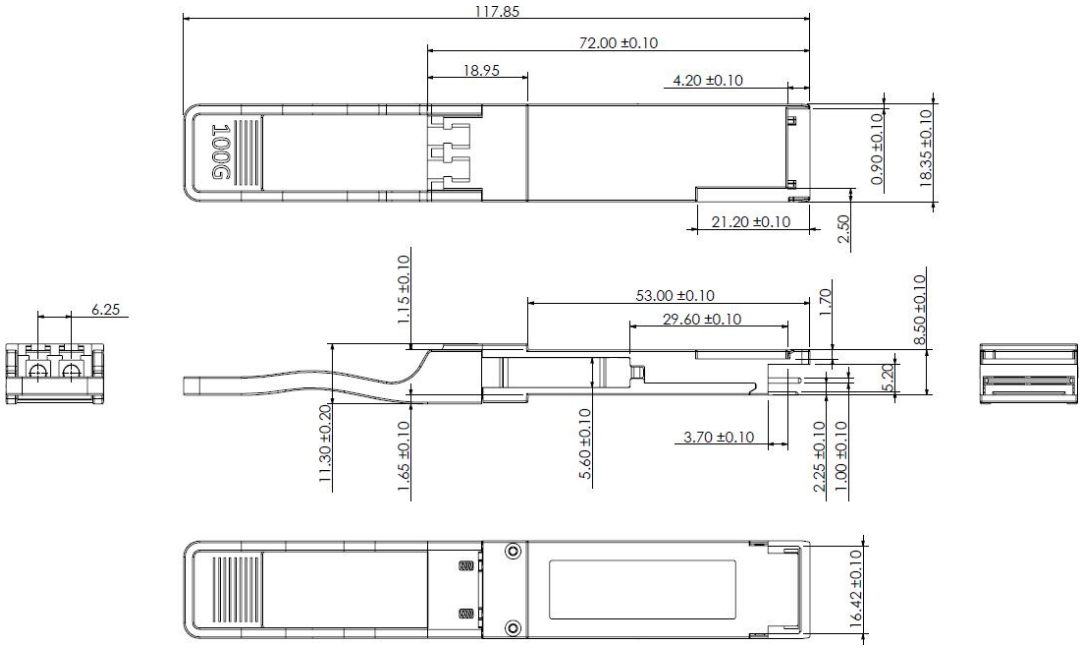
7 Recommended Power Supply Filter

The host board should use the power supply filtering as shown in the figure.



Recommended Power Supply Filter

8 Mechanical Dimensions



(Unit:mm[inch])

9 ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins,testedperMIL-STD-883,Method3015.4/JESD22-A114-A (HBM).However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

10 Ordering information

Part Number	Product Description
HD-QSFP28/100G-LR4	QSFP28 LR4 10km optical module with full real-time digital diagnostic monitoring And pulltab.

11 Document History

Version	Change Description	Changed by	Date
VERA	Initial Release	XuanXiao	26/03/2018
VERB	Update Optical Characteristics	Wang Xin	01/02/2021